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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/644,625	08/20/2003	Christopher A. Poirier	200208727-1	7519	
22879 7	7590 05/04/2006		EXAM.	EXAMINER	
HEWLETT PACKARD COMPANY			WHITMORE, STACY		
P O BOX 2724	400, 3404 E. HARMON JAL PROPERTY ADM	IY ROAD INISTRATION	ART UNIT	PAPER NUMBER	
INTELLECTU FORT COLLI	NS, CO 80527-2400	INISTRATION	2825		
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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	10/644,625	POIRIER ET AL.	
Office Action Summary	Examiner	Art Unit	
	Stacy A. Whitmore	2825	_,
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the	correspondence address	
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DATE of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  If NO period for reply is specified above, the maximum statutory period value to reply within the set or extended period for reply will, by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATIO 36(a). In no event, however, may a reply be til will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONI	N. nely filed I the mailing date of this communicati ED (35 U.S.C.§ 133).	
Status			
1) ☐ Responsive to communication(s) filed on <u>RCE</u> 2a) ☐ This action is <b>FINAL</b> . 2b) ☐ This  3) ☐ Since this application is in condition for allowal closed in accordance with the practice under E	action is non-final. nce except for formal matters, pr	osecution as to the merits	is
Disposition of Claims			
4)  Claim(s) 1-32 is/are pending in the application 4a) Of the above claim(s) is/are withdra 5)  Claim(s) is/are allowed. 6)  Claim(s) 1-32 is/are rejected. 7)  Claim(s) is/are objected to. 8)  Claim(s) are subject to restriction and/o	wn from consideration.		
Application Papers			
9) ☐ The specification is objected to by the Examine 10) ☑ The drawing(s) filed on 8/23/2003 is/are: a) ☑ Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) ☐ The oath or declaration is objected to by the E	accepted or b) objected to by drawing(s) be held in abeyance. S ction is required if the drawing(s) is c	ee 37 CFR 1.85(a). bjected to. See 37 CFR 1.12	1(d).
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:  1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Bureat * See the attached detailed Office action for a list	nts have been received. Its have been received in Applications Its documents have been received (PCT Rule 17.2(a)).	ation No ved in this National Stage	
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/06)  Paper No(s)/Mail Date	4) Interview Summa Paper No(s)/Mail 8) 5) Notice of Informa 6) Other:		

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## **DETAILED ACTION**

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3, 8-13, 16-21, 24-27, and 29-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Shakkarwar (US Patent 6,694,492).

As for claims 1-3, 8-13, 16-21, 24-27, and 29-32, Shakkarwar discloses the invention as claimed, including the system/ means for, method, and computer program product, having an IC on a VLSI die, and embedded micro-controller on the die adapted to monitor and control the VLSI environment to optimize the IC operation, and further monitors one or more of temperatures at one or more locations, power supplied to the IC, the IC power supply, clock frequency, power supply voltage, power supply current to the IC, fuse for providing hardware selection of parameters that are monitored, firmware, controlling the environment to optimize an IC operating power level/frequency to approach a design limit, reducing power supply voltage/clock frequency in response to over temperature; wherein said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit; said micro-controller detects a difference in temperatures between a plurality of locations in the IC and redistributes workload in response to said temperature difference [fig. 1, elements 130, 107, 137, 149, 139, 103; col. 3, lines 16-19, 34-36, 44-47; col. 4, lines 4-13, 20-54; col. 6, lines 34-62; col. 9, lines 26-29, 44-52; col. 10, lines 1-3, 22-29, and 59-62]; [fig. 1, as cited above in the rejection

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of claims 1, 8, and 16, and especially elements 130, 107, and 148, and col. 4, lines 4-54; and col. 6, lines 39-62. Shakkarwar discloses that the internal controller, element 130, (an embedded microcontroller) is able to monitor and control the operation of the integrated circuit via a thermal sensor or battery sensor as well as test vectors and/or user programming and/or diagnostic programming to adjust the operation of the integrated circuit in order to control things such as at least operating voltage or operating rate. Shakkarwar discloses in lines 4-19 that multiple areas under varying conditions (temperature variations and thermal management) of the integrated circuit are monitored and controlled by element 130 (embedded micro-controller).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 4, 14, 22, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shakkarwar (US Patent 6,694,492) in view of Rogenmoser (US Patent Application Publication 2003/0225999).
- 3. As for claims 4, 14, 22, and 28, Shakkarwar discloses the invention substantially as claimed, including the including the system/ means for, method, and computer program product, having an IC on a VLSI die, and embedded micro-controller on the die adapted to monitor and control the VLSI environment as cited above in the rejection of claim 1. Shakkarwar further discloses temperature sensor for the purpose of reducing operating frequency as cited in the rejection of claim 1.

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Shakkarwar does not specifically disclose the IC having two or more processor cores each with an integer and floating point unit and temperature sensors at each of the units or transferring a processing workload from one unit to another.

Rogenmoser discloses an having two or more processor cores each with an integer and floating point unit as well as reducing the operating frequency and transferring a processing workload from one unit to another [fig. 4, paragraphs 0057, 0064-0067; paragraphs 0045, 0048, 0049-0052].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shakkarwar and Rogenmoser because applying Shakkarwar's monitoring of temperature at each of the units for over temperature and transferring a processing workload from one unit to another would maintain a processor such as Rogenmoser's to within design limits for overheating which would meet restrictions for export [see Rogenmoser, paragraph 0064].

- 4. Claims 5, 15, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shakkarwar (US Patent 6,694,492) in view of Kim, K. (Korean Patent Publication 9405466 B1).
- 5. As for claims 5, 15, and 23, Shakkarwar discloses the invention substantially as claimed, including the including the system/ means for, method, and computer program product, having an IC on a VLSI die, and embedded micro-controller on the die adapted to monitor and control the VLSI environment as cited above in the rejection of claim 1. Shakkarwar further discloses monitoring and controlling current to the IC as cited above in the rejection of claim 1.

Shakkarwar does not specifically disclose ammeters comprising VCOs.

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Kim discloses ammeters comprising VCOs

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Shakkarwar and Kim because monitoring current levels with ammeters and VCOs would provide Shakkarwar's system with a way of determining current by utilizing voltage and resistance for calculation which would further aid Shakkarwar's system to determine over-temperature due to current levels.

6. Applicants arguments dated April 17, 2006, have been fully considered but they are not persuasive.

In the remarks, applicant argues in substance:

A: Shakkarwar or the combination of Shakkarwar and (Rogenmoser or Kim) does disclose including the system/ means for, method, and computer program product, having an IC on a VLSI die, and embedded micro-controller on the die adapted to monitor and control the VLSI environment to optimize the IC operation. wherein said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit; said micro-controller detects a difference in temperatures between a plurality of locations in the IC and redistributes workload in response to said temperature.

Examiner respectfully disagrees for the following reasons:

As to A: Shakkarwar or the combination of Shakkarwar and (Rogenmoser or Kim) does disclose including the system/ means for, method, and computer program product, having an IC on a VLSI die, and embedded micro-controller on the die adapted to monitor and control the VLSI environment to optimize the IC operation [fig. 1, as cited above in the rejection of claims 1, 8, and 16, and especially elements 130, 107, and

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148, and col. 4, lines 20-54; and col. 6, lines 39-62. Shakkarwar discloses that the internal controller, element 130, (an embedded microcontroller) is able to monitor and control the operation of the integrated circuit via a thermal sensor or battery sensor as well as test vectors and/or user programming and/or diagnostic programming to adjust the operation of the integrated circuit in order to control things such as at least operating voltage or operating rate; wherein said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit; said micro-controller detects a difference in temperatures between a plurality of locations in the IC and redistributes workload in response to said temperature difference [fig. 1, elements 130, 107, 137, 149, 139, 103; col. 3, lines 16-19, 34-36, 44-47; col. 4, lines 4-13, 20-54; col. 6, lines 34-62; col. 9, lines 26-29, 44-52; col. 10, lines 1-3, 22-29, and 59-62]; [fig. 1, as cited above in the rejection of claims 1, 8, and 16, and especially elements 130, 107, and 148, and col. 4, lines 4-54; and col. 6, lines 39-62. Shakkarwar discloses that the internal controller, element 130, (an embedded microcontroller) is able to monitor and control the operation of the integrated circuit via a thermal sensor or battery sensor as well as test vectors and/or user programming and/or diagnostic programming to adjust the operation of the integrated circuit in order to control things such as at least operating voltage or operating rate. Shakkarwar discloses in lines 4-19 that multiple areas under varying conditions (temperature variations and thermal management) of the integrated circuit are monitored and controlled by element 130 (embedded micro-controller).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore Primary Examiner Art Unit 2825

SAW

April 27, 2006